Cross-die timing methodology for Next-Gen Chiplet SoCs

A shift-left solution for cross-foundry 3DIC-STA Signoff

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62 THE CHIPS TO SYSTEMS CONFERENCE

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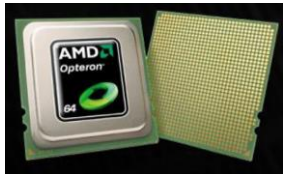
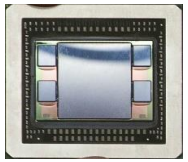
MOTIVATION

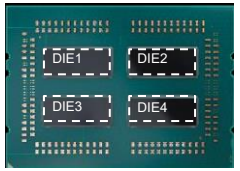
To keep the Moore's law alive, Chiplet with advance packaging are increasingly becoming the mainstream design choice. **CHIPLETS** are small modular chips packaged together, which if required can collectively work as a single unit.



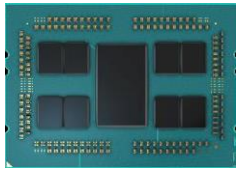
AMD: OPTERON



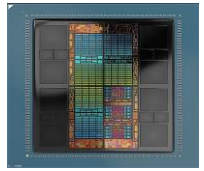
AMD: FIJI



AMD: EPYC, VEGA
INTEL: XEON, KABY LAKE



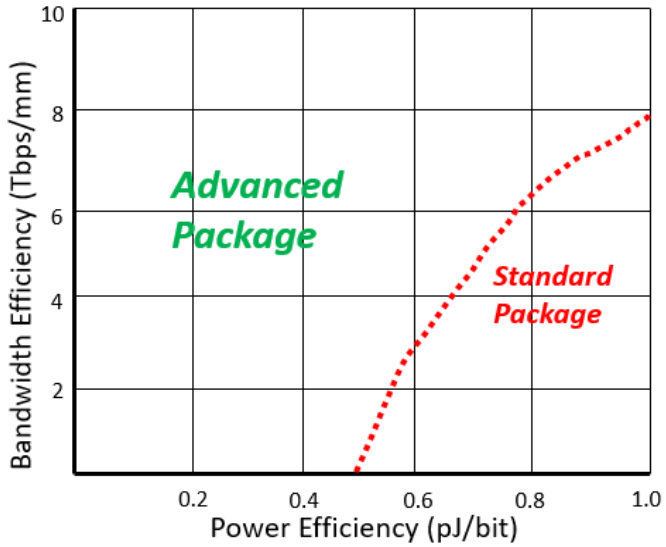
AMD: EPYC, NAVI
INTEL: LAKEFIELD
NVIDIA: AMPERE



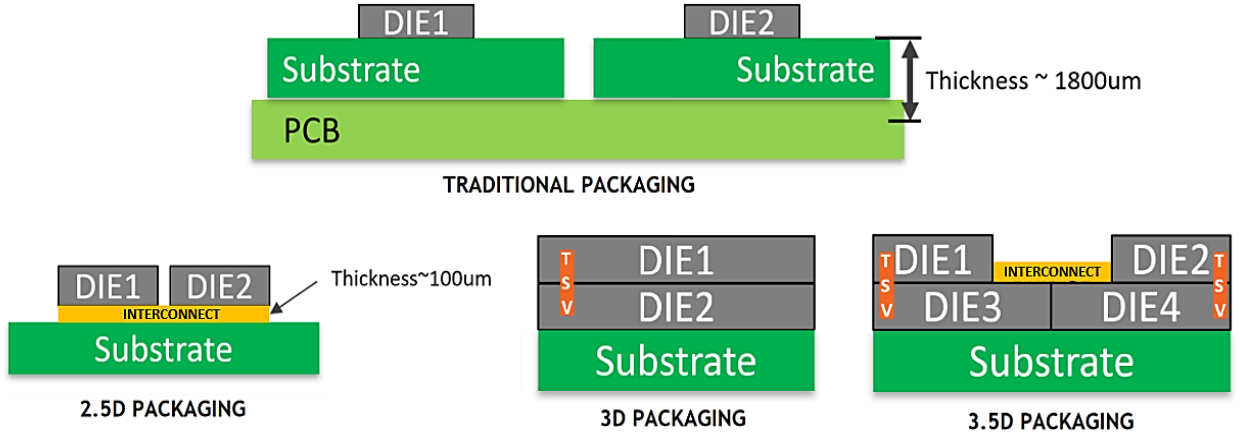
AMD: INSTINCT
INTEL: METEOR LAKE
NVIDIA: BLACKWELL

A generic Chiplet configuration includes multiple dies placed over a package substrate which provides connections to PCB, while an Interposer enables connections between dies and substrate.

MOTIVATION (CONTD.)



BANDWIDTH vs POWER EFFICIENCY TRENDS

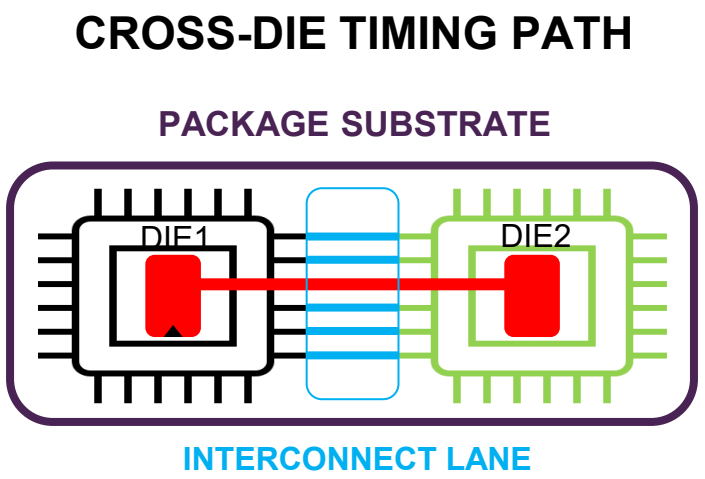


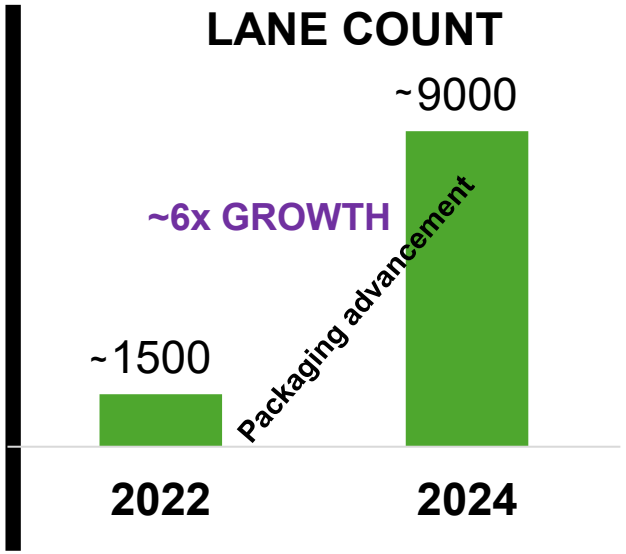
PACKAGING OPTIONS

- Advanced packaging techniques categorized as 2.5D, 3D & 3.5D Integration allows for higher die density while standardization of cross-die short reach PHY enables flexibility & interoperability to mix & match dies from different tech nodes or foundries altogether.
- Due to shorter interconnect distance, the dies can communicate using a simpler source-synchronous/clock-forwarding PHY architecture.

Cross-die/cross-tech timing closure scenario as the new ask of the hour.

CHALLENGES





- While link budgeting in terms of Signal Integrity/Power Supply Jitter analysis is still an integral part of sign-off; a low power PHY operating at low speed via short reach channel opens the possibility of cross-die STA + spice based margining methodology to become a substitute in future.

- The prime challenge to support the package level cross-die path timing becomes difficult as the lane count keeps increasing, thus paving more and more challenges to sign-off in single timing environment:

1. Formation of unit package level design netlist combining all dies within a single package.
2. Full-chip STA environment is complicated and has high run-time penalty; scaling to package level will not yield any return on investment.
3. All future cross-die path will be multi-tech-node type designs, which requires significant effort to setup flows and methodology.

Traditional signoff approaches do not catch-up with technology scaling trends.

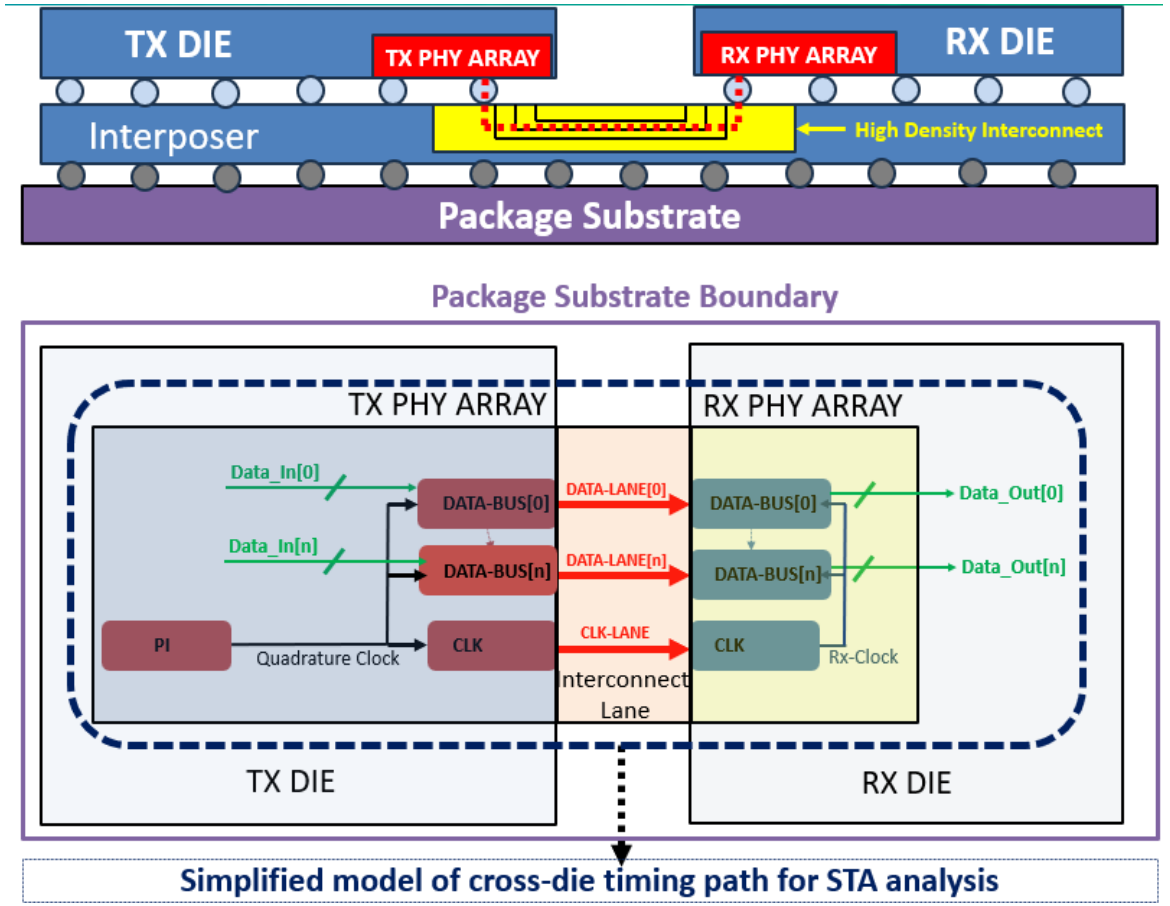
MAIN IDEA

- To address the above challenges, a novel “3DIC Cross-Die Static Timing Analysis & methodology” (3DIC-STA) with following elements is proposed :

A. **Simplified model of cross-die path:** Using reduced Transmitter (Tx) and Receiver (Rx) PHY logic placed at the chip boundary.

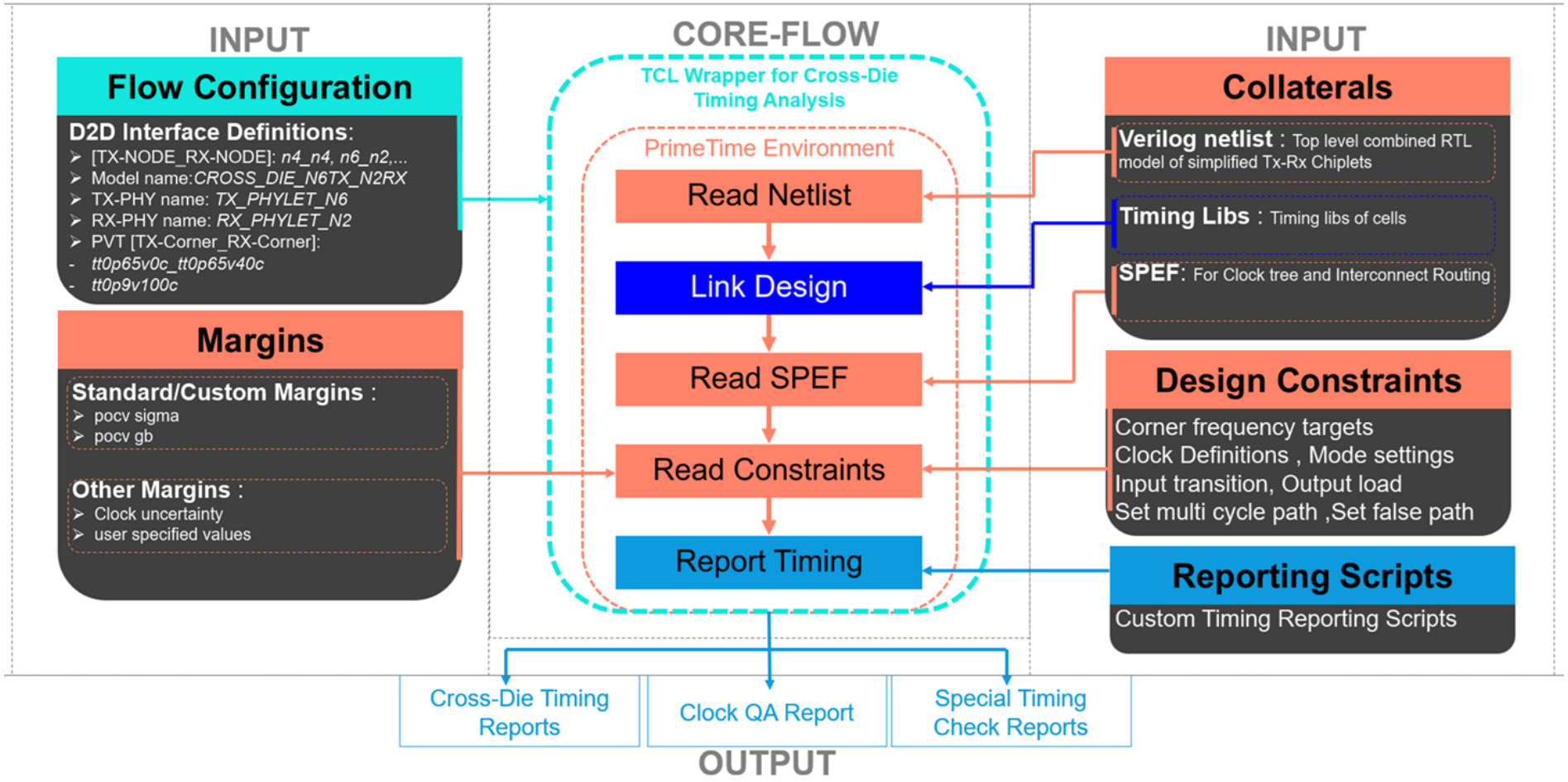
A. **Custom PrimeTime based cross-die flow:** We use the simplified model of cross-die timing paths to setup a package-level timing environment using a custom-built flow.

A. **SPICE based precise STA signoff margining:** Traditional STA pessimistic margining at full-chip level is not beneficial in terms of Power-Performance-Area (PPA). SPICE simulations models the variation and other non-linearity, which is then utilized for accurate margining in STA.



The proposal can be correlated with initial silicon results for future calibrations in production sign-off.

IMPLEMENTATION



A Generic, Scalable, Faster solution which required silicon data for correlation & sign-off confidence.

PERFORMANCE

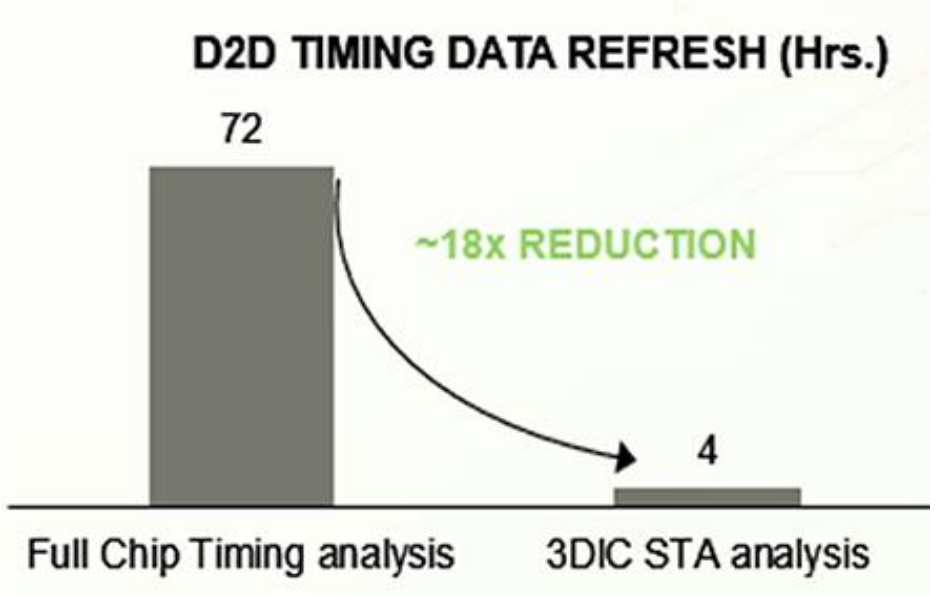
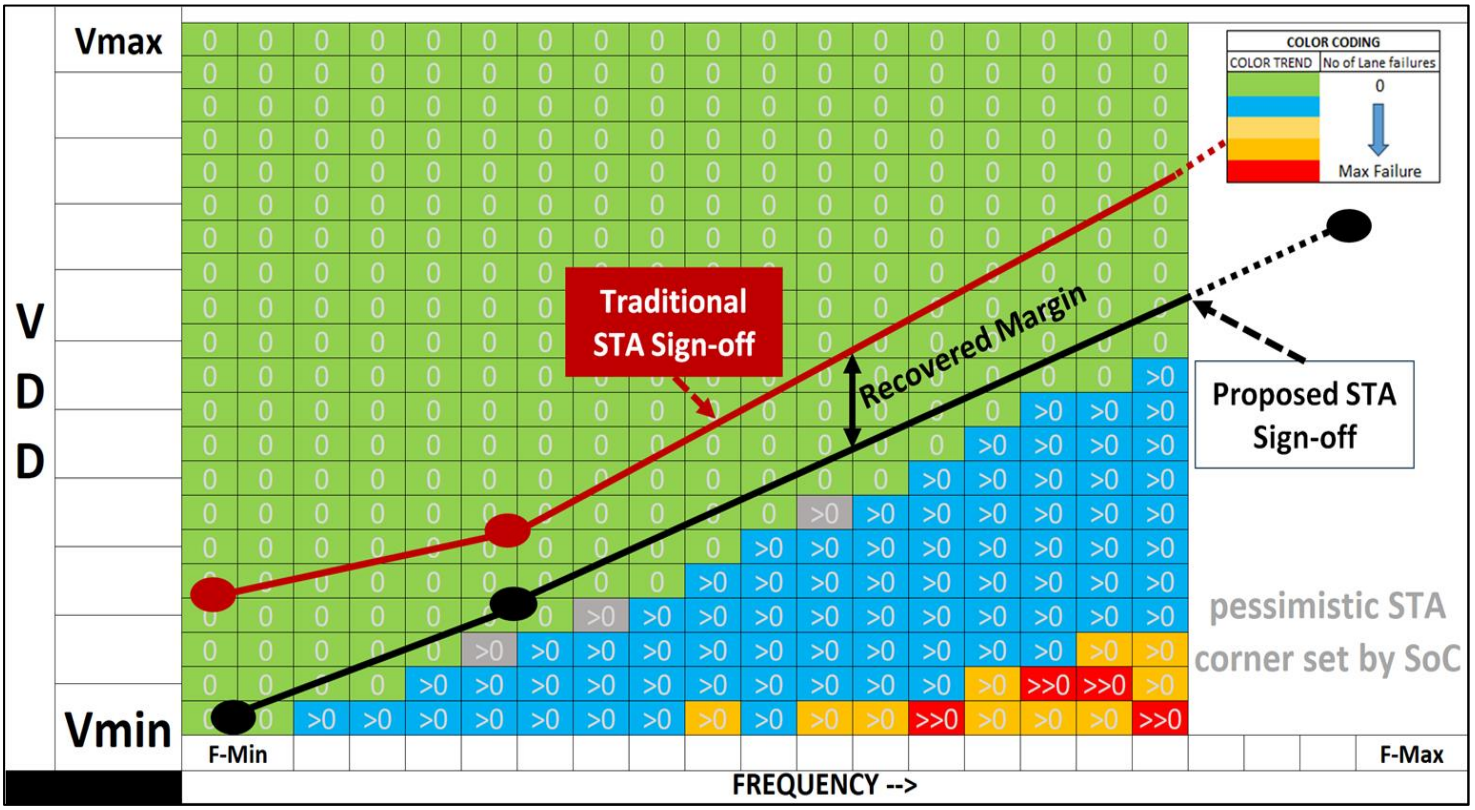


Figure describes the approximate run-time improvement as compared to an equivalent best-case analysis based on full-chip timing with respect to worst-case runtime with proposed 3DIC-STA solution – as is evident from the diagram we see a significant runtime improvement of approximately 18x (thanks to the simplified model explained in slide #6).

SILICON CORRELATION



SHMOO PLOT DESCRIBING SILICON CORRELATION WITH 3DIC-STA BASED SIGNOFF

Success of the silicon on a specific voltage-frequency (VF) is defined by number of lane failures. The data has been color coded for ease of visualization. The green area representing VF combination with **zero** lane failures, while the blue-orange-red area represents higher lane failures.

The proposed 3DIC-STA flow was also successful in recovering hidden margins in the design.

All lane failures are observed beyond the STA target range, thereby establishing accuracy of the 3DIC STA Solution. Further, the difference between RED & BLACK line shows the STA margins that were recovered leading to better performance per watt.

FUTURE WORK

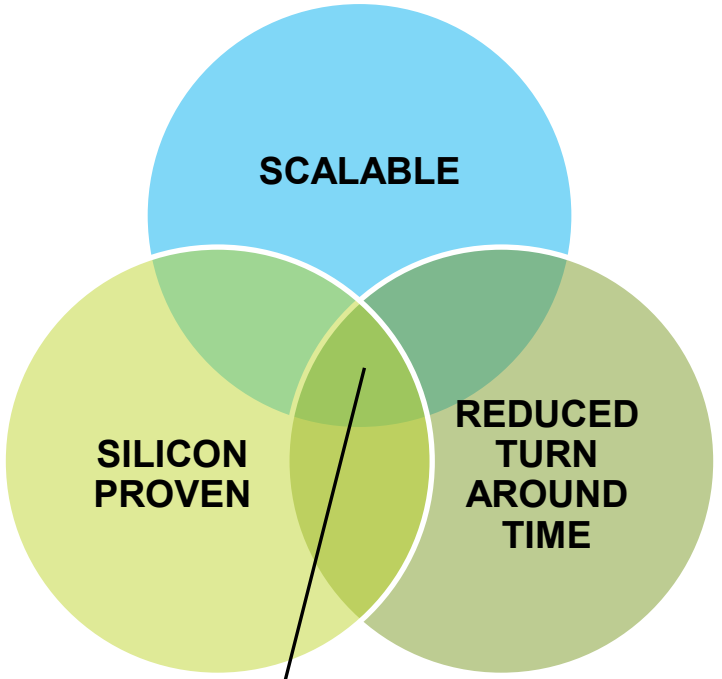
- There's a trend of consistent increase in die-to-die lane count, which will further accelerate with higher stacking density. It will result in significant increase in die-to-die source-synchronous paths, which is a prefect application for the proposed 3DIC-STA Solution for package level co-design.

- The proposed methodology can be further improved for future package-level co-design requirements with following areas of improvement:

AUTOMATED CIRCUIT REDUCTION	AUTOMATED CORRELATION WITH FULL CHIP TIMING	PACKAGE LEVEL CO-DESIGN ENHANCEMENT	TIMING BUDGETING BASED SIGN-OFF
CREATE SIMPLIFIED MODEL OF CROSS-DIE PATHS FOR ALL LANES.	TO ALLOW EFFICIENT CORRELATION WITH FULL CHIP TIMING.	EXTEND TO OTHER SIGNOFF AREAS SUCH AS THERMAL, STRESS & RELIABILITY.	AUTOMATED CROSS-DIE BUDGETING BASED SIGNOFF; ENABLING BOARD LIKE PLUG-AND-PLAY CONVENIENCE.

CONCLUSION

- Following are the novelty elements associated with cross-die STA solution:
  - Industry leading package level die-to-die STA flow supporting signoff across processes, technology nodes and foundries.
  - Scalable to in-package die-to-die interfaces of various lane/array sizes.
  - Silicon proven Signoff accuracy aided by SPICE based precise margining, leading to extra margin recovery.
  - Faster turn-around time compared to a monolithic full-chip STA run due to efficient reduction of database.



Enabling shift-left capability to pre-fetch full-chip issues

Q&A